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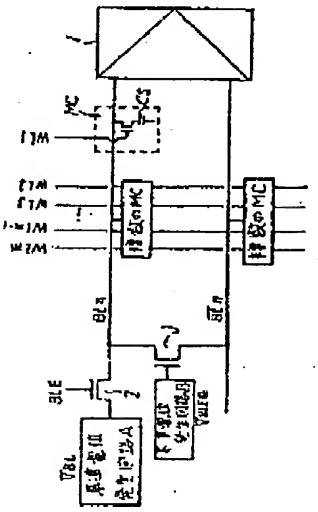
TITLE : SEMICONDUCTOR MEMORY DEVICE



ABSTRACT : PURPOSE: To quickly obtain a memory cell with a small margin and to attain the shortening of testing time by transmitting different reference potential to two bit lines connected to respective sense amplifiers.

CONSTITUTION: Plural bit lines MLn and the inverse of BLn (n=1...n) are connected to a sense amplifier 1. Respective memory cells MC include a transfer gate and a capacity Cs for which the information of an H level or an L level is accumulated. To the gate of the transfer gate of the plural memory cells MC, word lines WLm (1...m) are connected to cross to the bit line. Besides, an n-type FET 2 is connected between the bit line MLn and a reference potential generating circuit A and the gate is connected to an input signal BLE. Besides, for an n-type FET 3, the gate is connected to a reference potential generating circuit B. By this constitution, a potential difference between the bit lines becomes large on H reading and small on L reading and by making it close to the amplifiable minimum potential difference, the testing time can be shortened.